DOCUMENT-IDENTIFIER: US 6239042 B1
TITLE: Process for realizing an intermediate dielectric layer for enhancing the planarity in semiconductor electronic devices

---------- KWIC ---------

DWKU:
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APD:
19971209

BSPR:
In fact, non-volatile memories require that an N-doped insulating dielectric layer be provided to promote electric charge retention in the gate regions associated with the memory cells by the well-known mechanism of gettering the movable metal ions into a dielectric including the N dopant. A first known approach to meeting this requirement for optimized planarity within the above constraints is shown in FIGS. 1A and 1B, and provides for the deposition of an insulating dielectric layer of the BPSG type between the semiconductor substrate and the overlying metallization plane using a PECVD technique from a gaseous or a solid source. Planarization is then completed by a thermal treatment in an oven at temperatures close to the melting temperature of the deposited dielectric layer.

BSPR:
The second planarizing layer is formed by depositing, from a liquid source, a material of the SOG type containing silicates and no organic radicals. Such silicates may be lightly doped with phosphorus. These materials are evenly spread over the first dielectric layer by a "spinning" technique, and then solidified by thermal treatments which result in the materials polymerizing at low temperatures, barely higher than 400.degree. C. After that, these materials are stabilized by a thermal treatment with temperatures higher than 700.degree. C. To seal this intermediate dielectric layer, as a potential cause for diffusion of impurities into the substrate, a third dielectric layer, typically of silicon oxide, is deposited by chemical vapor deposition techniques (PECVD, APCVD, SACVD, etc.). This third layer must be doped with impurities of either the N or Phosphorous type to meet the requirements for charge retention to the memory cells integrated on the semiconductor substrate (gettering of movable metal impurities).

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438/780

CCXR:
438/781

CCXR:
438/789

CCXR:
438/790

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DOCUMENT-IDENTIFIER: US 5963837 A

TITLE: Method of planarizing the semiconductor structure
DATE-ISSUED: October 5, 1999

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APPL-NO: 8/ 846924
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US-CL-CURRENT: 438/760,438/633 ,438/698 ,438/699 ,438/762 ,438/763

FIELD-OF-SEARCH: 438/760;438/762 ;438/763 ;438/626 ;438/631 ;438/633 ;438/634
;438/697 ;438/698 ;438/699

REF-CITED:

U.S. PATENT DOCUMENTS

PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL
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5312512	May 1994	Allman et al.	156/636
5449314	September 1995	Meikle et al.	438/699
5534731	July 1996	Cheung	257/759

ART-UNIT: 283

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ABSTRACT:
A method for planarizing a semiconductor structure having a first surface region with a high aspect ratio topography and a second surface region with a low aspect ratio topography. A flowable material is deposited over the first and second surface regions of the structure. A portion of the material fills gaps in the high aspect ratio topography to form a substantially planar surface over the high aspect ratio topography. A doped layer, for example phosphorus doped glass, is formed over the flowable oxide material. The doped layer is disposed over the high aspect ratio and over the low aspect ratio regions. Upper surface portions over the low aspect ratio region are higher than an upper surface of the flowable material. The upper portion of the doped layer is removed over both the first and second surface portions to form a layer with a substantially planar surface above both the high aspect ratio region and the low aspect ratio region. The method is used for filling gaps, such as gaps between adjacent gate electrodes formed in a gate electrode surface region of a semiconductor structure.

14 Claims, 4 Drawing figures
Exemplary Claim Number: 1
Number of Drawing Sheets: 2

BRIEF SUMMARY:
BACKGROUND OF THE INVENTION

This invention relates generally to integrated circuits and manufacturing methods and more particularly to structures and methods having improved planarity and alkali ion gettering properties.

As is known in the art, in forming small line width geometries in a semiconductor process using photolithography, it is necessary to provide a highly planar surface for various photolithographic masks used in such process. Further, in the fabrication of dynamic random access memories (DRAMs), a plurality of gate electrodes are formed adjacent one another with relative small separation, i.e., gaps, between each adjacent pair thereof. The plurality of gate electrodes provide a high aspect ratio topography.

Further, the surface region adjacent the high aspect ratio topography may be relative low, i.e., relatively flat. Thus, it is necessary to fill these gaps width a suitable material, preferably a material with a low dielectric constant

to prevent coupling between the adjacent electrodes and provide a planar surface over both the high and low aspect ratio topographies for subsequent photolithography.

With one process, after the gate electrodes are formed, a dielectric layer of silicon nitride is chemically vapor deposited (CVD) over the surface. The CVD silicon nitride is a conformal deposition and therefore gaps remain between adjacent gate electrode structures. The gap width between gate electrode structures after the layer of silicon nitride is deposited is in the order of 1200 .ANG.. Next, a layer of borophosphorosilicate glass (BPSG) is chemically vapor deposited over the structure to fill in the gaps. The CVD BPSG is thick enough to not only fill the gaps but also extends over the tops of the CVD silicon nitride layer and over the filled gaps to a thickness in the order of 1000 .ANG..

As is also known in the art, contaminants, such as sodium ions, or other alkali ions may come into contact with the outer BPSG layer. However, the phosphorous in the BPSG layer acts as a gettering material to counteract the effect of the alkali ion contaminant. The structure is then heated to form a more planar surface. However, with aspect ratios of 3-5 or higher, the BPSG layer may not provide a surface with the requisite degree of planarity.

SUMMARY OF THE INVENTION

In accordance with the invention, planarizing a semiconductor structure having a first surface region with a high aspect ratio topography and a second surface region with a low aspect ratio topography is provided. A material is deposited over the first and second surface regions of a substrate. A portion of material fills gaps in the high aspect ratio topography to form a substantially planar surface over the high aspect ratio topography, the levels of the high and low aspect ratio topographies over the surface of the substrate being different. A doped layer, for example phosphorus doped glass, is formed over the deposited material. The doped layer is disposed over the high aspect ratio and over the low aspect ratio regions. Upper surface portions of the doped layer over the low aspect ratio region are higher than an upper surface of the deposited material. The upper surface portions of the doped layer are removed over both the first and second surface portions to form a doped layer with a substantially planar surface above both the high and low aspect ratio topographies.

In accordance with another feature of the invention, a method for filling gaps between adjacent gate electrodes formed in a gate electrode surface region
of a semiconductor structure is provided. The method includes the step of

spinning on a material over the structure. A first portion of such material flows between the gate electrodes to fill the gaps and a second portion of such material becomes deposited over tops of the gate electrodes and over the gaps to form a layer with a substantially planar surface over the gate electrodes. A doped layer, for example phosphorus doped glass, is formed over the self-planarizing material. An upper portion of the doped layer is removed to form a layer with a substantially planar surface above the region of the gate electrode surface region of the semiconductor structure.

The invention provides a substantially planar layer over the semiconductor structure for subsequent photolithography and the phosphorous dopant provides gettering to remove adverse effects of alkali contaminant ions which may enter the doped layer. Still further, the dielectric constant of the material filling the gaps, i.e., the first portion of the gap filling material, being substantially free of such contaminants and dopant, has a relatively low dielectric constant thereby reducing electrical coupling between adjacent electrodes.

In accordance with one feature of the invention, the spin-deposited material is a flowable material, such as hydrogensilsesquioxane glass. The phosphorous doped layer may be provided by chemical vapor deposition, for example.

DRAWING DESCRIPTION:
BRIEF DESCRIPTION OF THE DRAWING

Other features of the invention, as well as the invention itself, may be more fully understood with reference to the following detailed description taken together with the accompanying drawings, in which:

FIGS. 1-4 are diagrammatical, cross sectional sketches of a semiconductor integrated circuit structure fabricated in accordance with the invention; FIG. 1 showing a plurality of gate electrodes disposed over a high aspect ratio topography surface region of a semiconductor substrate such region adjacent a low aspect ratio topography surface region; FIG. 2 showing the structure of FIG. 1 after such structure having spun over it a self-planarizing material, a first portion of such material flowing between the gate electrodes to fill the gaps and a second portion of such material becoming deposited over tops of the gate electrodes and over the gaps to form a layer with a substantially planar surface; FIG. 3 showing the structure after a doped layer is deposited over the self-planarizing material; and FIG. 4 showing a the structure after the doped layer is planarized over both the high and low aspect ratio topographies.

DETAILED DESCRIPTION:
DETAILED DESCRIPTION

Referring now to FIG. 1, a semiconductor substrate 10, here a silicon wafer, is provided. As shown, a plurality of MOS transistors 12 has been formed on the upper surface thereof. Each one of the transistors 12 has source and drain regions, not shown, with a corresponding one of a plurality of gate electrodes 14 disposed between each of the source and drain regions. Here, each gate electrode 14 includes a bottom layer 16 of thermally grown silicon dioxide, a layer 18 of doped, low pressure chemical vapor deposited (LP CVD) polycrystalline silicon formed on the silicon dioxide layer 16, a layer 20 of chemically vapor deposited tungsten-silicide formed on the polycrystalline silicon layer 18 and a top layer 21 of silicon nitride. The height H' of the gate stack (i.e., layers 16, 18, 20, and 21) is here about 4000 .ANG.. After forming the gate stack, a silicon nitride liner 22 is chemically vapor deposited over surface of the structure. Here, the silicon nitride liner 22 has a thickness of about 300 .ANG.. Further, here the length (L) of the gate electrodes 14 (i.e., the across the outer sidewalls of the silicon nitride liner 22) is in the order of 1800 .ANG. and the space (S) or gaps 28 between adjacent gate electrodes 14 (i.e., the distance between the outer sidewall of the adjacent silicon nitride liners 22) is in the order of about 1200 .ANG.. It is noted that the surface of the structure shown in FIG. 1 has a high aspect ratio region 23 where the gate electrodes 14 are formed and a low aspect ratio region 25. The aspect ratio is the ratio of the height of the topography to the width of the topography. The aspect ratio (A) is the ratio of H' to S (i.e., A=H'/S). Here, in the high aspect ratio region 23, A is in the range from about 3.3 to 4.1 or higher. It is noted that in the low aspect ratio region 25, A is substantially zero.

After patterning the gate electrodes 14 using conventional photolithographic etching techniques, a self-planarizing material 27 is spun over the surface of the structure, as shown in FIG. 2. The material 27 is a flowable material. In one embodiment, the flowable material is an oxide such as hydrogensilsesquioxane glass manufactured and sold by Dow-Corning, Midland, Mich. When such flowable oxide material 27 is spun on the wafer, it is self-planarizing and a first, lower portion 26 of the material 24 flows between the gate electrodes 14 to fill the gaps 28 between adjacent gate electrodes 14 and a second, upper portion 29 of the material 24 becomes deposited over tops of the gate electrodes 14 and the filled gaps 28 between adjacent gate electrodes 14 to form a layer 30 with a substantially planar surface portion 32a over the aspect ratio region 23 and substantially planar surface 32b over the low 32b aspect ratio region 25; it being noted that there is a non-planar transition region 32 between regions 32a, 32b. That is, the surface portions 32a, 32b are at different heights above the surface of the substrate 10.

The self-leveling material 26 is deposited in a thickness to sufficiently

provide isolation between the gate stacks and conductive layer (not shown) above the self-leveling material. In one embodiment, the thickness (T) of the self-leveling material over the low aspect ratio region 25 is in the order of about 3000 .ANG.. The thickness of the material 26 in region 29 is about 1000 .ANG. and about 5000 .ANG. in the region 26. After spin-depositing the material 24, the structure is baked on a hot plate and cured in an oven at about 400.degree. C. for about one hour in a nitrogen atmosphere to harden the material.

Referring to FIG. 3, a layer 36 is provided over the upper surface of the cured material 24. The layer is doped with an alkali ion gettering dopant 31, such as phosphorous. The dopant concentration of phosphorous in the layer is sufficient to getter contaminants. The dopant concentration, in one embodiment, is about 2-6 weight %, preferably about 2-5 weight %, and more preferably about 2-4 weight %. The doped layer, for example, is phosphorous doped silicate glass (PSG) formed by chemical vapor deposition (CVD). The formation of PSG by CVD results in a conformal layer, causing the height of the surface portion 33a of layer 36 over the high aspect ratio region 23 to be greater than the height of surface portion 33b of layer 36 over the low aspect ratio region 25. It is also noted that height of the surface portion 32b of layer 36 is greater than the height of the surface portion 32a of the material 27. That is, upper surface portion 33b of the doped layer 36 over the low aspect ratio region 25 are higher than the upper surface portions 32a, 32b of the flowable oxide material 27. The layer 36 is sufficiently thick such that the upper surface portion 33b is higher than the upper surface portion 32a. As shown, the doped layer 36 is deposited to a thickness of about 4000 .ANG..

Referring now to FIG. 4, portions of the upper surfaces 33a, 33b (FIG. 3) of the doped layer are removed by, for example, chemical mechanical polishing (CMP). The CMP produces a doped layer 36 with a substantially planar surface 33c above both the high and low aspect ratio topographies and over the non-planar transition region 32. The doped layer above the high aspect ratio topographies is sufficiently thick to effectively getter contaminants. In one embodiment, the thickness of the doped layer in the high aspect ratio topographies is about 1000 .ANG..

Thus, with the methods described above, a structure shown in FIG. 4 is highly planar as required for subsequent photolithographic processing, for example in forming upper metalization layers or electrically conductive interconnecting wires (not shown). Further, the phosphorous dopant provides gettering to remove adverse effects of alkali ion contaminant ions. Still further, the dielectric constant of the material filing the gaps 28, being substantially free of such contaminants, has a relatively low dielectric constant (i.e., in the order of 3.0 to 3.8) thereby reducing electrical

coupling between adjacent gate electrodes.

Other embodiments are within the spirit and scope of the appended claims. For example, other flowable materials may be spun-on the structure shown in FIG. 1, such as spun-on silica aerogel or other inorganic spun on materials. Still further, the flowable material may be formed using a gaseous deposition process with similar flow properties as that obtained with the spun on glass material described above instead of using such spin deposited process. One such material which may be used with gaseous deposition is Flowfill material sold by PMT-Electrotech, Chatsworth, Calif. Still further, the process may be used to fill gaps other then gaps between adjacent gate electrodes, such as gaps between metal lines used as electrical interconnects over the structure.

CLAIMS:

What is claimed is:

1. A method for planarizing a semiconductor structure having a first surface region of a substrate with a high aspect ratio topography and a second surface region of the substrate with a low aspect ratio topography, such method comprising the steps of:

depositing a flowable material over the first and second surface regions of the substrate, such material being characterized in that after deposition the material has a substantially planar surface, a portion of the material filling gaps in the high aspect ratio topography of the first surface region and forming a substantially planar surface over the high aspect ratio topography first surface region and a substantially planar surface over the low aspect ratio second surface region, the planar surface over the first surface region being at a different level over the substrate than the planar surface over the second surface region; and

forming a doped layer over the deposited flowable material, the doped layer being formed over the high aspect ratio and over the low aspect ratio first and second surface regions, upper surface portions of the doped layer over the low aspect ratio second surface region being higher than upper surface portions of the deposited flowable material over the high aspect ratio first surface regions; and

removing upper surface portions of the doped layer over both the first and second surface portions to form the doped layer with a substantially planar surface, such planar surface of the doped layer extending above both the first and second surface regions.

2. The method recited in claim 1 wherein the step of forming the doped

layer comprises the step of chemical vapor depositing phosphorus doped glass.

3. The method recited in claim 1 wherein the step of depositing the flowable material comprises the step of spin depositing such flowable material.

4. The method recited in claim 1 wherein the step of depositing the flowable material comprises the step of using gaseous deposition.

5. The method recited in claims 1, 2 or 3 wherein the step of depositing the flowable material comprises the step of depositing a flowable oxide.

6. The method recited in claim 3 wherein the spin depositing step comprises the step of spin depositing hydrogensilsesquioxane glass.

7. The method recited in claims 1, 2 or 3 wherein the step of depositing the flowable material comprises the step of depositing a flowable inorganic material.

8. A method for planarizing a semiconductor structure having a first surface region of a substrate with a high aspect ratio topography and a second surface region of the substrate with a low aspect ratio topography, such method comprising the steps of:

depositing a flowable material over the first and second surface regions of the substrate, such material being characterized in that after deposition the material has a substantially planar surface, a portion of such material filling gaps in the high aspect ratio topography of the first surface region forming a substantially planar surface over the high aspect ratio topography first surface region and a substantially planar surface over the low aspect ratio second surface region, the planar surface over the first surface region being at a different level over the substrate than the planar surface over the second surface region; and

curing the flowable material;

forming a doped layer over the cured flowable material, the doped layer being formed over the high aspect ratio and over the low aspect ratio first and second surface regions, upper surface portions of the doped layer over the low aspect ratio second surface region being higher than upper surface portions of the deposited flowable material over the high aspect ratio first surface regions; and

removing upper surface portions of the doped layer over both the first and second surface portions to form the doped layer with a substantially planar

surface, such planar surface of the doped layer extending above both the first and second surface regions.

9. The method recited in claim 8 wherein the step of forming the doped layer comprises the step of chemical vapor depositing phosphorus doped glass.

10. The method recited in claim 8 wherein the step of depositing the flowable material comprises the step of spin depositing such flowable material.

11. The method recited in claim 8 wherein the step of depositing the flowable material comprises the step of using gaseous deposition.

12. The method recited in claims 8, 9 or 10 wherein the step of depositing the flowable material comprises the step of depositing a flowable oxide.

13. The method recited in claim 10 wherein the spin depositing step comprises the step of spin depositing hydrogensilsesquioxane glass.

14. The method recited in claims 8, 9 or 10 wherein the step of depositing the flowable material comprises the step of depositing a flowable inorganic material.

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TITLE: Polishstop planarization method and structure
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REF-CITED:

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ART-UNIT: 114

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ABSTRACT:
The invention provides a method for producing a substantially planar surface overlying features of a semiconductor structure. The method comprises forming alternating layers of a hard polishing material and a soft polishing material over the features of the semiconductor structure, and then polishing the alternating layers to form a substantially planar surface over the features. The method takes advantage of the polish rates of the various materials used as alternating layers to enhance the planarization process.

24 Claims, 14 Drawing figures
Exemplary Claim Number: 11
Number of Drawing Sheets: 4

BRIEF SUMMARY:
TECHNICAL FIELD

This invention relates to a planarization method and structure, more particularly to a method which utilizes polishstops to create a substantially planar surface. In the method, alternating layers of hard and soft polishing materials are utilized to take advantage of their respective polish rates so that planarization of the alternating layers is enhanced or controlled.

BACKGROUND ART

Integrated circuits generally have a system of metallized interconnects which couple the various devices fabricated in a semiconductor substrate. Typically, aluminum or some other metal is deposited and then patterned to form interconnect paths along the surface of the silicon substrate. In most processes, a dielectric or insulative layer is then deposited over this first metal layer, via openings are etched through the dielectric layer, and a second metallization layer is deposited. The second metal layer covers the dielectric layer and fills the via openings, thereby making electrical contact down to the first metal layer. The purpose of the dielectric layer is to act as an insulator between the first metal layer and the second metal layer interconnects.

Most often, the intermetal dielectric layer comprises a chemical vapor deposition (CVD) of silicon dioxide. This silicon dioxide layer covers the first metal interconnects conformably so that the upper surface of the silicon dioxide layer is characterized by a series of non-planar steps which correspond in height to the underlying first metal lines.

These step-heights in the upper surface of the interlayer dielectric have several undesirable features. First, a non-planar dielectric surface interferes with the optical resolution of subsequent photolithographic processing steps. This makes it extremely difficult to print high resolution lines. A second problem involves the step coverage of the second metal layer over the interlayer dielectric. If the step height is too large, there is a serious danger that open circuits will be formed in the second metal layer.

To combat these problems, various techniques have been developed in an attempt to better planarize the upper surface of the interlayer dielectric. One approach, known as chemical mechanical polishing, employs abrasive polishing to remove the protruding steps along the upper surface of the dielectric. According to this method, the silicon substrate is placed face down on a table covered with a pad which has been coated with an abrasive material, also known as a polishing compound or slurry. Both the wafer and the table are then rotated relative to each other to remove the protruding portions. This abrasive polishing process continues until the upper surface of the dielectric layer is largely flattened.

Current all-polish planarization schemes are severely limited because polish rates are strong functions of feature sizes. For any polishing pad, narrow down areas polish more slowly than wide down areas, which are slower than wide
up areas, which are slower than narrow up areas. "Down" areas refer to recessed portions of the semiconductor structure, and "up" areas refer to raised portions of the semiconductor structure. Up areas are often formed by the metallization lines referred to above, leaving the unoccupied silicon substrate surface as the down area. "Wide" up areas often occur as a result of a dense array pattern of metallization, while "narrow" up areas occur as a result of isolated metallization lines. Achieving a final planarized surface becomes a balancing act between several different polish rates and initial thicknesses of these wide and narrow up and down features.

Current back end of line (BEOL) planarization processes use either a simple dielectric polish or add a hard top polish layer. Modelled results for one example of an all oxide polish are shown in Table 1. This data is for a specific process with a specific pad. For the all oxide polish, a balancing act between the polishing non-uniformities and the feature size polish rate dependencies exist. Wider down areas planarize much more slowly than narrower
down areas. More material must be removed to achieve planarity. When the step
height associated with the 0.1 mm down feature is reduced to 1390 Angstroms,

the differences in step heights between 0.1 and 0.5 mm down features exceed 1000 Angstroms with 20,000 Angstroms of material removed, leaving 2300 Angstroms of topographical variation due to typical polishing non-uniformities. Clearly, this simple oxide polishing process is not effective for planarization for down area feature sizes greater than 0.1 mm.

TABLE 1 _____ Modelling results for a
simple oxide polish (Suba 500) Step Height [= A].sup.4 Down Area Distance [= mm] Amt 3- down Pol.sup.1 0.1 0.5 1.5 sigma.sup.2 range.sup.3
_____ 1000 7329 7571 7753 120 424 3000 6153
6783 7284 360 1131 6000 4732 5751 6632 720 1900 10000 3334 4615 5852 1200
2518 15000 2153 3505 5006 1800 2853 20000 1390 2662 4282 2400 2892 40000 241
886 2292 4800 2051 75000 11 129 767 9000 756
_____ .sup.1 Amount of material polished
and/or removed from uparea .sup.2 3sigma polishing uniformity of 12% in amount
of expected variation .sup.3 Variation in down area step heights from 1.5 mm to .1 mm .sup.4 Step height calculated from model for down area dimensions and
amounts removed as noted

In regard to placing a hard upper layer on the polished material, this offers a significant improvement. This process does not control dishing over wide metal lines, however, as no polishstop is present in these areas. Therefore, this process does not allow for over polishing to eliminate the approximate 2500 Angstroms of incurred polishing non-uniformities, in addition to feature size dependencies discussed above.

In addition, simple polish planarization processes cannot deal with diverse metallization densities, such as where wide unpatterned areas cover half of the chip and dense patterns cover the other half. For these applications, such single polish planarization processes will fail because non-planarities accumulate from level to level leading to such problems as tungsten puddling and problems associated with long contact and via overetches. This results in difficulties in photolithography, film deposition over steps, and via etching.

Thus, in spite of attempts at obtaining globally planarized surfaces, a need still exists for a method of obtaining such planarized surfaces while overcoming the problems discussed above.

DISCLOSURE OF INVENTION

This need is met, and the problems of the prior methods overcome, by the methods and structures of the subject invention. Briefly, the invention provides a method for producing a substantially planar surface over features of a semiconductor structure. The features include raised and recessed portions, for example metal lines and trenches. Alternating layers of a hard polishing material and a soft polishing material are formed over the features of the semiconductor structure. These alternating layers are then polished so as to create the substantially planar surface. The polishing takes advantage of the different polish rates of the alternating layers to achieve such global substantial planarity as an end result. The structures of the invention are used to enhance the properties of a chemical mechanical polish to enhance planarity and allow control of the polishing process.

Suitable soft polishing materials include dielectrics, such as silicon dioxide, phosphosilicate glass (PSG), borophosphosilicate glass (BPSG), sputtered quartz, and polyimide. Suitable hard polishing materials include silicon nitride, silicon carbide, diamond like carbon, alumina, tungsten, and silicon dioxide. Silicon dioxide can be used as the hard polishing material when the soft polishing material is BPSG or PSG. "Hard" and "soft" polishing materials as used herein derive meaning in the context of being relative to one another. A hard polishing material polishes more slowly than a soft polishing material, under similar polishing conditions.

The invention also provides a substantially planar surface formed by alternating layers of hard and soft polishing materials which surround tungsten vias. The top surface of the filled vias forms a portion of the planar surface, eliminating problems such as tungsten puddling.

DRAWING DESCRIPTION:

BRIEF DESCRIPTION OF DRAWINGS

The foregoing and other objects, features and advantages of the invention will be apparent from the following more particular description of preferred embodiments of the invention as illustrated in the accompanying drawings in which:

FIG. 1 is a cross-section side elevational view of an initial structure according to one embodiment of the subject invention;

FIG. 2 is a cross-section side elevational view of the structure shown in FIG. 1 after polishing to remove portions of the top slowly polishing material;

FIG. 3 is a cross-section side elevational view of the structure shown in FIG. 2 after further polishing to remove the dielectric overlying the metal lines;

FIG. 4 is a cross-section side elevational view of the structure shown in FIG. 3 after further polishing or wet etching to remove the remaining slowly polishing material;

FIG. 5. shows step height and required silicon nitride as a function of feature size and the amount of dielectric removed, normalized to initial step height.

FIG. 6 is a cross-section side elevational view of an initial structure according to a further embodiment of the subject invention;

FIG. 7 is a cross-section side elevational view of the structure shown in FIG. 6 after the first polishing to remove the top slowly polishing material and the underlying dielectric overlying the metal lines;

FIG. 8 is a cross-section side elevational view of the structure shown in FIG. 7 after a selective dip to remove the exposed polishstop;

FIG. 9 is a cross-section side elevational view of the structure shown in FIG. 8 after a second polish to remove the dielectrics;

FIG. 10 is a cross-section side elevational view of the structure shown in FIG. 9 after further polishing or wet etching to remove the exposed polishstop;

FIG. 11 is a cross-section side elevational view of an initial structure according to a further embodiment of the subject invention;

FIG. 12 is a cross-section side elevation view of the structure shown in FIG. 11 after photolithography and via etch;

FIG. 13 is a cross-section side elevational view of the structure shown in FIG. 12 after tungsten deposition and etchback; and

FIG. 14 is a cross-section side elevational view of the structure shown in FIG. 13 after polishing which removes the upper dielectric, eliminating tungsten puddling and providing a polishstop.

DETAILED DESCRIPTION:
BEST MODE FOR CARRYING OUT THE INVENTION

As mentioned previously, the broad concept of the subject invention is directed to a method for producing a substantially planar surface overlying features of a semiconductor structure. The method provides for planarity enhancement and/or control by utilizing chemical-mechanical polishing of at least three alternating layers of hard and soft materials, e.g. hard-soft-hard or soft-hard-soft, over the interlayer dielectric. As conformal layers, the hard and soft layers each rise and fall with the contour of the semiconductor structure. This creates up and down areas of each hard and soft layer.

To understand the concept of the subject invention, consider alternating hard/soft/hard layers. The hard layer overlying the interlayer dielectric is considered a buried polishstop layer. This polishstop layer allows for an overpolish without reverse dishing problems, so that planarity can be achieved. The upper hard layer is of a thickness such that it will remain in the widest "down" areas when planarization is achieved. The middle soft layer is of a thickness to align the top and bottom layers, allowing for overpolish.

The embodiment described in the above paragraph is known as the "leveling internal polishstop". This embodiment utilizes a buried polishstop layer in conjunction with a hard upper layer, to obtain enhanced planarization.

Referring to FIG. 1, the "leveling internal polishstop" starting structure consists of hard/soft/hard layers overlying the interlayer dielectric of a semiconductor structure. The semiconductor substrate 10 as shown has metal lines 12 on its surface. The alternating layers of hard and soft polishing materials overlie interlayer dielectric 14 covering the metal lines 12 and surface 13 of the substrate 10. Sequentially from top to bottom, the alternating layers comprise a hard polishing material 20, a soft polishing material 18, and a hard polishing material 16 overlying the interlayer dielectric 14. In this embodiment, the hard polishing material 16 acts as the buried polishstop layer to prevent overpolishing or reverse dishing. This allows for enhancement of planarization. For some applications, the hard polishing material 16 and interlayer dielectric 14 may be combined into one layer, provided the material polishes significantly slower than the other soft polishing material 18 above it.

As shown in FIG. 2, the hard polishing material 20 has been polished away over the raised features, i.e. the metal lines 12. This exposes the underlying layer of soft polishing material 18 overlying the raised features. Polishing is continued to remove the soft polishing material 18 overlying the raised features, so that the hard polishing material 16 is exposed (see FIG. 3). At this time, the hard polishing material 20 overlying the recessed areas and the hard polishing material 16 overlying the raised areas form a substantially

planar surface.

FIG. 4 shows an optional embodiment in which the remaining hard polishing material 20 has been removed by polishing or wet etching. This results in the soft polishing material 18 overlying the recessed areas and the hard polishing material 16 overlying the raised areas forming the substantially planar surface.

A more detailed discussion of the embodiment shown in FIGS. 1-4 is provided below. For the purposes of the discussion, the following materials will be used: the top hard polishing material will be silicon nitride, the top soft polishing material will be PSG, and the lower hard polishing material and interlayer dielectric will be combined into one silicon dioxide film.

In the first polish step, the top silicon nitride layer acts to maintain the selectivity between the up and down area polish rates. Silicon nitride polishes 4-5 times more slowly than PSG. Consequently, the step between the up
and down areas is effectively maintained while an equivalent of 4 times as much PSG has been removed. This minimizes the polish rate of the down areas.

This polishstep can be modelled quantitatively to evaluate the polishing performance and to establish the necessary film thickness of slowly polishing materials and of the polishstop. A semi-empirical model was used, which incorporates dishing data, in conjunction with the understanding that relative polish rates of up and down features are a linear function of the step height between features.

Modelled results presented in FIG. 5 show graphically the reduction in step height for four down area feature sizes relative to a wide up area as a function of the amount of material removed (after the hard upper layer has been polished off of the features and assuming that the polish stop remains in all the down areas). The lower plot shows the required amount of silicon nitride consumed during the polish in the down areas. Silicon nitride well in excess of 2000 Angstroms is necessary for feature sizes of 500 .mu.m or greater, for this characterized CMP process. Differences in the amount of silicon nitride consumed as a function of feature size severely limit the final planarity of the structure.

For processing, step heights of 8000 Angstroms are typical. With 2500 Angstroms of silicon nitride and 8000 Angstroms of PSG being removed during the
polish, and approximately 14% 3-sigma polishing uniformity, 2500 Angstroms of surface non-uniformity will result. To compensate, an overpolish is necessary.

Because silicon dioxide polishes 40% slower than PSG, 750 Angstroms of additional silicon dioxide should be added as a polishstop. The resulting structure will consist of, from bottom to top: 3750 Angstroms of silicon dioxide, 7250 Angstroms of PSG, and 2500 Angstroms of silicon nitride. The final surface above the lower topography will be planar to +/-750 Angstroms in addition to the non-uniformities discussed above.

This modeling data is for a specific process and a specific pad, and represents one example of the enhancement of planarity. The method of the subject invention can be used with any polishing process to enhance the performance of the planarization process. For example, if a planarization process can achieve a range of 2 mm, that process can be enhanced to obtain a range of 5 mm. If another planarization process can achieve a range of 5 mm, the process can be enhanced utilizing the method of the subject invention to achieve a range of 8 mm, for example. Thus, the modeling example given is merely to illustrate the enhancement of the planarization obtainable with the given process and pad by utilizing the method of the subject invention.

In a further embodiment of the subject invention, known as the "sacrificial oxide and polishstop", the range of planarity achievable with the "leveling internal polishstop" is extended. This is accomplished by using polishing to selectively reveal up area films (hard layers), then selectively removing the hard layer and polishing to planarity. Polishing is first used to expose an upper buried hard polishstop layer over "up" areas of the semiconductor structure. A selective etch is then used to remove the upper hard polishstop over the "up" areas without etching of the underlying soft polishing material. A second polish then removes the soft polishing material, leaving the upper hard polishstop over the "down" areas and the lower hard polishstop over the "up" areas. A planar surface results.

Referring to FIG. 6, the "sacrificial oxide polishstop" starting structure consists of hard/soft/hard/soft/hard layers overlying the interlayer dielectric of a semiconductor structure. The semiconductor substrate 22 as shown has metal lines 24 on its surface 23. The alternating layers of hard and soft polishing materials overlie interlayer dielectric 26 covering the metal lines 24 and surface 23 of the substrate 22. The starting structure consists of a sacrificial first hard polishstop 36, soft polishing material layers 30 and 34, and hard polishing material layers 28 and 32 overlying the interlayer dielectric 26. Examples of combinations of common materials which can be used
for each alternating layer are outlined in Table 2.

TABLE 2 _____ Model of Step Height for

Current Polishing Art Possible Dielectric/Polishstop/Selective dip Combinations _____ Top level/Slowly polishing
materials Si.sub.3 N.sub.4, Diamond like Carbon Second level down Dielectric Polishstop Selective Dip PSG, TEOS, SiO.sub.2 Si.sub.3 N.sub.4 Hot Phosphoric Acid PSG, TEOS, BPSG, SiO.sub.2 Al.sub.2 O.sub.3 Nitric Acid Bottom Layers Dielectric Polishstop PSG SiO.sub.2 PSG, BPSG, TEOS, SiO.sub.2
Si.sub.3 N.sub.4 _____

A more detailed discussion of the embodiment shown in FIGS. 6-10 is provided
below. For the purposes of the discussion, the following materials will be used: the first two hard polishstops 32 and 36 are silicon nitride and PSG is used for the dielectric 26 and the soft polishing material layers 30 and 34. The final polishstop 28 will be silicon dioxide. The structure is polished to remove the hard polishing material 36 and the soft polishing material 34 overlying the raised features. Polishing continues until the tops of the polishstop layer 32 are exposed (see FIG. 7), while the down areas remain covered by PSG due to the relative polish rates of up and down areas. Next, the exposed polish stop 32 is selectively removed (see FIG. 8) and the structure is polished flat using both the silicon dioxide final polishstop 28 and the silicon nitride polishstop 32 as polishstops (see FIG. 9). An optional step can then be used to selectively remove the remaining silicon nitride polishstop 32 by polishing or wet etching techniques (see FIG. 10).

Critical to the above described process is the understanding that the maximum allowable dishing length or range for the above mentioned process is on
the order of 2 mm for the modelled example given, which is large for the dimensions common to logic chip down areas compared to the 0.1 mm range in the
same modelled process discussed in the background. The second polish uses the
remaining silicon nitride and silicon dioxide as polish stops. After this polish, the silicon nitride is removed selectively and the silicon dioxide remains. For subsequent RIE processing for interlevel contacts and vias, silicon dioxide and PSG etch nearly identically.

In the first polish step, the top silicon nitride layer acts to maintain the selectivity between up and down area polish rates. Silicon nitride polishes 4 times more slowly than silicon dioxide. Consequently, the step between the up and down areas is effectively maintained while an equivalent of 4 times as much silicon dioxide has been removed, thus minimizing the polish rate of the down

areas.

The dimensions or range at which this invention will provide substantial planarization can be calculated using process characterization curves [Burke, VLSI Metallization and Interconnect Conference Proceedings, pp. 379-383 (1991)]. Calculations are made by first calculating the ratio between "up" and "down" polish rates where the first buried polish stop/hard layer will be exposed after the first polish. This "critical ratio" can be calculated, as governed by the following equation:

Critical ratio=[1-(Ox.sub.top /FT)]/(1+unif/2).sup.2.

Ox.sub.top is the critical amount of oxide which is required to protect the polish stop layer from the subsequent removal step and FT and unif represent the thickness of the top nitride/dielectric layers and the polishing uniformity respectively. A down area with more than Ox.sub.top of dielectric left over the polish stop before the selective removal step will be protected from dishing in the subsequent polish. With approximately 14% 3 sigma uniformity, using a 7% overpolish and 160 nm of silicon nitride and 300 nm of silicon dioxide, a ratio of down to up area polish rates must be 0.85 or less to leave 30 nm of oxide. Given this critical ratio, the process characterization curve is used to translate the ratio into a range for the given process. For a Suba-500 pad (see Burke reference), the largest allowable "down" area would be
in excess of 3.6 mm. This critical ratio data is for the process illustrated. As with the modeling example, the equation can be utilized with other polishing processes to determine the range attainable with a particular characterized process and pad combination.

However, most chip designs do not have large unpatterned up areas, but instead have large patterned areas which polish faster than the model systems. Allowances for array patterning need to be made for processing and computing critical ranges. Arrays with pattern factors less than 1 after deposition will give faster "up" rates and hence enhance the performance of the invention.

The second polish step is timed to remove the dielectric over the final polishstop. This process has polishstop in the down area and polishstop above the lower topography (metal lines), which allows for a significant over-polish to combat polishing non-uniformities with little risk of reverse dishing in both the down areas and the areas above the lower topography. This feature ends the balancing act common for prior art planarization processes and allows for a more manufacturable process. The Sacrificial oxide and polishstop process as described in this Example will consistently leave the same amount of dielectric above the lower topography.

The advantages of this embodiment of the subject invention thus include the ability to achieve a planar surface to within 1000 Angstroms in a reproducible and controllable fashion with minimal risk of reverse dishing or of over/underpolishing (which are common problems for current planarization processes). The method will also work for chip patterns which represent the realm of possible logic designs, while current art will fail to meet a 1000 Angstroms planarization goal. Current polishing art cannot planarize effectively for down area dimensions greater than 0.5 mm while models and experimental results demonstrate that the subject invention planarizes effectively in excess of 2 mm, for the example given. As discussed above, this enhancement of planarity is attainable with other polishing processes. In relative terms, a "poor" polishing process can be enhanced to a "fair" polishing process, or a "fair" polishing process can be enhanced to a "good" process. Similarly, a "good" polishing process can be enhanced to a "great" polishing process.

In an additional embodiment of the subject invention, known as "tungsten-interlevel dielectric and stud with a leveling internal polishstop planarization", planarity is controlled to convert a "down" area having residual tungsten to an "up" area. This allows for polishing to a planar surface without polishing away tungsten studs, while eliminating residual tungsten.

Referring to FIG. 11, the tungsten-interlevel dielectric starting structure is shown to include a semiconductor substrate 38 upon the surface 39 of which are located metal lines 40. The structure further consists of several alternating hard and soft materials, including sequentially from top to bottom: an approximately 200 nm of soft polishing dielectric 50, a hard polishing material 48 (about 200 nm), about 760 nm of soft polishing dielectric 46, and about 80 nm of hard polishstop 44 overlying roughly 1800 nm of interlevel dielectric 42. For some applications, the final hard polishstop 44 and interlevel dielectric 42 may be combined into one layer, provided the material polishes significantly slower than the other soft polishing dielectric material above it 46.

After deposition of the alternating hard and soft layers, vias 52 are etched as shown in FIG. 12. Because the vias 52 are all on the same level, all etch distances are approximately the same and a severe overetch is not necessary. A
1:1 dielectric:silicon nitride via etch presents no current technical problems.

Next, tungsten 54 is deposited and etched back, filling the majority of the vias 52, leaving no more than a 1200 nm seam, as shown in FIG. 13. The

structure is then polished as illustrated in FIG. 14. With the addition of 200 nm of dielectric above 200 nm of polishstop, tungsten puddling will be eliminated. This dielectric essentially holds any residual tungsten up above the polishstop, and allows for the easy and complete removal of the tungsten. The sequence of polishstops will allow for improved planarity over current simple oxide polishing and for a significant overpolish.

As a working example, the following materials can be used: the slowly polishing materials will be silicon nitride and the top two dielectrics will be PSG and the lower interlevel dielectric will be silicon dioxide.

The invention thus provides for the addition of a polishstop layer and an upper dielectric layer, which makes the process more controllable but also solves many inherent problems with current art such as allowing for an extended range of polishing planarity, ending tungsten puddling, and ending "China Syndrome". The invention also results in considerable process savings by eliminating two processing steps and by developing a larger process window.

While the invention has been particularly shown and described with reference to preferred embodiments thereof, it will be understood by those skilled in the art that various changes in form and details may be made therein without departing from the spirit and scope of the invention.

CLAIMS:

We claim:

1. A method for producing a substantially planar surface overlying features of a semiconductor structure, which method comprises:

forming alternating layers of a hard polishing material and a soft polishing material over features of a semiconductor structure, said features including raised and recessed portions, wherein said alternating layers comprise a conformal first layer of a hard polishing material overlying said features of said semiconductor structure, a conformal second layer of a soft polishing material overlying said first layer of a hard polishing material, and a conformal third layer of a hard polishing material overlying said second layer of a soft polishing material, and wherein said first layer comprises silicon dioxide, said second layer comprises phosphosilicate glass, and said third layer comprises silicon nitride; and

polishing said alternating layers so as to create a substantially planar surface over said features.

2. A method for producing a substantially planar surface overlying features

of a semiconductor structure, which method comprises:

forming alternating layers of a hard polishing material and a soft polishing material over features of a semiconductor structure, said features including raised and recessed portions, wherein said alternating layers comprise:

a conformal first layer of a hard polishing material overlying said features of said semiconductor structure;

a conformal second layer of a soft polishing material overlying said first layer of a hard polishing material;

a conformal third layer of a hard polishing material overlying said second layer of a soft polishing material;

a conformal fourth layer of a soft polishing material overlying said third layer of a hard polishing material; and

a conformal fifth layer of a hard polishing material overlying said fourth layer of a soft polishing material; and

polishing said alternating layers so as to create a substantially planar surface over said features.

3. The method of claim 2 wherein said first layer comprises silicon dioxide, said second and fourth layers each comprise phosphosilicate glass, and said third and fifth layers each comprise silicon nitride.

4. The method of claim 2 wherein said polishing comprises:

polishing said fifth layer to reveal said fourth layer;

polishing said fourth layer positioned over said raised portions so as to reveal said third layer positioned over said raised portions;

removing said third layer positioned over said raised portions so as to reveal said second layer positioned over said raised portions; and

polishing said fourth layer positioned over said recessed portions so as to reveal said third layer positioned over said recessed portions, and polishing said second layer positioned over said raised portions to reveal said first layer positioned over said raised portions,

wherein said third layer positioned over said recessed portions and said

first layer positioned over said raised portions form the substantially planar surface over said features.

5. The method of claim 4 wherein removing said third layer comprises etching selective for said third layer.

6. The method of claim 4 further comprising removing said third layer positioned over said recessed portions so as to reveal said second layer positioned over said recessed portions, wherein said second layer positioned over said recessed portions and said first layer positioned over said raised portions form the substantially planar surface over said features.

7. The method of claim 6 wherein removing said third layer comprises etching selective for said third layer or polishing said third layer.

8. A method for producing a substantially planar surface overlying features of a semiconductor structure, which method comprises:

forming alternating layers of a hard polishing material and a soft polishing material over features of a semiconductor structure, said features including raised and recessed portions, wherein said alternating layers comprise:

a conformal first layer of a hard polishing material overlying said features of said semiconductor structure;

a conformal second layer of a soft polishing material overlying said first layer of a hard polishing material; and

a conformal third layer of a hard polishing material overlying said second layer of a soft polishing material; and

polishing said alternating layers so as to create a substantially planar surface over said features, wherein said polishing comprises:

polishing said third layer positioned over said raised portions so as to reveal said second layer positioned over said raised portions; and

polishing said second layer positioned over said raised portions so as to reveal said first layer positioned over said raised portions,

wherein said third layer positioned over said recessed portions and said first layer positioned over said raised portions form the substantially planar surface over said features.

9. The method of claim 8 further comprising polishing said third layer positioned over said recessed portions so as to reveal said second layer positioned over said recessed portions, wherein said second layer positioned over said recessed portions and said first layer positioned over said raised portions form the substantially planar surface over said features.

10. A method for producing a substantially planar surface overlying features of a semiconductor structure, which method comprises:

sequentially, in an unbroken sequence, forming alternating layers of a hard polishing material and a soft polishing material over features of a semiconductor structure, said features including raised and recessed portions, wherein said alternating layers comprise:

a conformal first layer of a soft polishing material overlying said features of said semiconductor structure;

a conformal second layer of a hard polishing material overlying said first layer of a soft polishing material;

a conformal third layer of a soft polishing material overlying said second layer of a hard polishing material;

a conformal fourth layer of a hard polishing material overlying said third layer of a soft polishing material; and

a conformal fifth layer of a soft polishing material overlying said fourth layer of a hard polishing material; and

polishing said sequentially formed alternating layers so as to create a substantially planar surface over said features.

11. A method for producing a substantially planar surface overlying features of a semiconductor structure, which method comprises:

forming alternating layers of a hard polishing material and a soft polishing material over features of a semiconductor structure, said features including radioed and recessed portions, wherein said alternating layers comprise:

a conformal first layer of a soft polishing material overlying said features of said semiconductor structure;

a conformal second layer of a hard polishing material overlying said first layer of a soft polishing material;

a conformal third layer of a soft polishing material overlying said second layer of a hard polishing material;

a conformal fourth layer of a hard polishing material overlying said third layer of a soft polishing material;

a conformal fifth layer of a soft polishing material overlying said fourth layer of a hard polishing material; and

a conformal sixth layer of a hard polishing material overlying said fifth layer of a soft polishing material; and

polishing said alternating layers so as to create a substantially planar surface over said features.

12. The method of claim 11 wherein said polishing comprises:

polishing said sixth layer to reveal said fifth layer;

polishing said fifth layer positioned over said raised portions so as to reveal said fourth layer positioned over said raised portions;

removing said fourth layer positioned over said raised portions so as to reveal said third layer positioned over said raised portions; and

polishing said fifth layer positioned over said recessed portions so as to reveal said fourth layer positioned over said recessed portions, and polishing said third layer positioned over said raised portions to reveal said second layer positioned over said raised portions,

wherein said fourth layer positioned over said recessed portions and said second layer positioned over said raised portions form the substantially planar surface over said features.

13. The method of claim 12 wherein removing said fourth layer comprises etching selective for said fourth layer.

14. The method of claim 12 further comprising removing said fourth layer positioned over said recessed portions so as to reveal said third layer positioned over said recessed portions, wherein said third layer positioned over said recessed portions and said second layer positioned over said raised portions form the substantially planar surface over said features.